**CLAIMS**:

1. A board on chip package, comprising:

an insulative substrate having circuitry thereon and an opening therethrough;

a semiconductive-material-comprising die adhered to the substrate and electrically connected to the circuitry with a plurality of electrical interconnects extending through the opening; and

a metal foil in physical contact with at least a portion of the die.

2. The board on chip package of claim 1 wherein the foil is adhered to the substrate with an electrically conductive epoxy.

3. The board on chip package of claim 1 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with only a portion of said second surface.

4. The board on chip package of claim 1 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with an entirety of said second surface.

5. The board on chip package of claim 1, wherein the die has a first surface facing the substrate, a second surface in opposing relation to the first surface, and a sidewall between the first and second surfaces, the foil being adhered to the substrate proximate the sidewall and extending across the sidewall to physically contact the second surface.

6. The board on chip package of claim 5 wherein the sidewall has a length, and wherein the foil physically contacts a predominate portion of the sidewall length.

7. The board on chip package of claim 5 wherein the sidewall has a length, and wherein the foil is spaced from a predominate portion of the sidewall length by a gap.

8. The board on chip package of claim 5 wherein the sidewall has a length, wherein the foil is spaced from a predominate portion of the sidewall length by a gap, and wherein the gap has electrically conductive epoxy extending from the sidewall to the foil.

9. The board on chip package of claim 5 wherein the sidewall has a length, wherein the foil is spaced from a predominate portion of the sidewall length by a gap, and wherein the gap is filled with electrically conductive epoxy extending from the sidewall to the foil.

10. The board on chip package of claim 1 wherein the metal foil is selected from the group consisting of copper foil and aluminum foil.

11. The board on chip package of claim 1 wherein the die is adhered to the substrate with an electrically conductive epoxy.

12. A board on chip package, comprising:

an insulative substrate having circuitry thereon and an opening therethrough;

a semiconductive-material-comprising die adhered to the substrate and electrically connected to the circuitry with a plurality of electrical interconnects extending through the opening; and

a metal foil adhered to a portion of the die with an electrically conductive adhesive.

13. The board on chip package of claim 12 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with only a portion of said second surface.

14. The board on chip package of claim 12 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with an entirety of said second surface.

15. The board on chip package of claim 12 wherein the die has a first surface facing the substrate, a second surface in opposing relation to the first surface, and a sidewall between the first and second surfaces, the foil being adhered to the substrate proximate the sidewall and extending across the sidewall to physically contact the second surface.

16. The board on chip package of claim 15 wherein the sidewall has a length, and wherein the foil physically contacts a predominate portion of the sidewall length.

17. The board on chip package of claim 15 wherein the sidewall has a length, and wherein the foil is spaced from a predominate portion of the sidewall length by a gap.

18. The board on chip package of claim 15 wherein the sidewall has a length, wherein the foil is spaced from a predominate portion of the sidewall length by a gap, and wherein the gap has electrically conductive epoxy extending from the sidewall to the foil.

19. The board on chip package of claim 15 wherein the sidewall has a length, wherein the foil is spaced from a predominate portion of the sidewall length by a gap, and wherein the gap is filled with electrically conductive epoxy extending from the sidewall to the foil.

20. The board on chip package of claim 12 wherein the metal foil is selected from the group consisting of copper foil and aluminum foil.

21. A board on chip package, comprising:

an insulative substrate having circuitry thereon and an opening therethrough;

a semiconductive-material-comprising die adhered to the substrate and electrically connected to the circuitry with a plurality of electrical interconnects extending through the opening, the die having a first surface facing the substrate, a second surface in opposing relation to the first surface, and a sidewall surface extending between the first and second surfaces; and

a thermally conductive material in physical contact with at least two of the die first surface, second surface and sidewall surface; the thermally conductive material having a thermal conductivity under specified conditions equal to or greater than the thermal conductivity of elemental copper under the same specified conditions.

22. The board on chip package of claim 21 wherein the thermally conductive material comprises a silver-filled epoxy.

23. The board on chip package of claim 21 wherein the thermally conductive material comprises a metal foil.

24. The board on chip package of claim 21 wherein the thermally conductive material comprises a material selected from the group consisting of aluminum foil and copper foil.

25. The board on chip package of claim 21 wherein the thermally conductive material is in physical contact with the second surface.

26. The board on chip package of claim 21 wherein the thermally conductive material is in physical contact with the sidewall and the second surface.

27. The board on chip package of claim 21 wherein the thermally conductive material is in physical contact with the sidewall, the first surface and the second surface.

28. A board on chip package, comprising:

an insulative substrate having circuitry thereon and an opening therethrough, the substrate comprising a first surface and a second surface in opposing relation to the first surface, the circuitry being on the first surface, the substrate further comprising a cavity extending into the second surface and proximate the opening;

a semiconductive-material-comprising die received within the cavity and electrically connected to the circuitry with a plurality of conductive interconnects extending through the opening, the die having an inner surface facing the substrate and an outer surface in opposing relation to the inner surface; and

a metal sheet in physical contact with at least a portion of the die outer surface.

29. The board on chip package of claim 28 wherein the die is entirely received in the cavity inwardly of the second surface of the substrate, and wherein the sheet extends along the second surface of the substrate and over the cavity to enclose the die in the cavity.

30. The board on chip package of claim 28 wherein the metal sheet is selected from the group consisting of copper foil and aluminum foil.

31. The board on chip package of claim 28 wherein the die is adhered to the substrate with an electrically conductive epoxy.

32. A board on chip package, comprising:

an insulative substrate having a pair of opposing surfaces and an opening extending therethrough, the opposing surfaces being a first surface and a second surface;

circuitry on the first surface of the substrate;

a semiconductive-material-comprising die adhered to the second surface of the substrate, the die having a pair of opposing surfaces, one of the die opposing surfaces being a first die surface and being aligned to face toward the second surface of the substrate, the other die surface being a second die surface and being aligned to face away from the second surface of the substrate, the die further comprising first and second opposing sidewalls extending between the first and second surfaces;

electrical interconnects extending from the die, through the opening and to the circuitry;

a metal foil contacting the substrate at a first location proximate the first sidewall and a second location proximate the second sidewall, the metal foil extending across the first and second sidewalls and over the second die surface; the metal foil physically contacting a predominate portion of the second die surface.

33. The board on chip package of claim 32 wherein the metal foil comprises a foil selected from the group consisting of aluminum foil and copper foil.

34. The board on chip package of claim 32 wherein the foil is adhered to the substrate with an electrically conductive epoxy.

35. The board on chip package of claim 32 wherein the foil is in physical contact with only a portion of the second die surface.

36. The board on chip package of claim 32 wherein the foil is in physical contact with an entirety of the second die surface.

37. The board on chip package of claim 32 wherein the sidewall has a length, and wherein the foil physically contacts a predominate portion of the sidewall length.

38. The board on chip package of claim 32 wherein the sidewall has a length, and wherein the foil is spaced from a predominate portion of the sidewall length by a gap.

39. The board on chip package of claim 32 wherein the sidewall has a length, wherein the foil is spaced from a predominate portion of the sidewall length by a gap, and wherein the gap has electrically conductive epoxy extending from the sidewall to the foil.

40. The board on chip package of claim 32 wherein the die is adhered to the substrate with an electrically conductive epoxy.

41. The board on chip package of claim 32 wherein the die comprises a rectangular outer periphery having four sides, wherein the metal foil extends outwardly beyond the outer periphery of the die and contacts the substrate at locations proximate each of the four sides.

42. A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough;

adhering a semiconductive-material-comprising die to the substrate with an electrically conductive adhesive, the die having circuitry supported thereby; and

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening.

43. The method of claim 42 wherein the electrically conductive adhesive comprises silver-filled epoxy.

44. The method of claim 42 wherein the die has a surface, and further comprising placing a metal foil in physical contact with at least a portion of the die surface.

45. A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough;

adhering a semiconductive-material-comprising die to the substrate and electrically connecting circuitry supported by the die with the circuitry on the substrate utilizing a plurality of electrical interconnects extending through the opening; and

joining a metal foil to the substrate, the metal foil having a segment extending over the die and in physical contact with at least a portion of the die.

46. The method of claim 45 wherein the joining the metal foil to the substrate comprises welding the metal foil to the substrate by melting a portion of the metal foil with a portion of the substrate.

47. The method of claim 46 wherein the melting is accomplished with a laser.

48. The method of claim 45 wherein the joining the metal foil to the substrate comprises adhering the metal foil to the substrate with an electrically conductive epoxy.

49. The method of claim 45 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with only a portion of said second surface.

50. The method of claim 45 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with an entirety of said second surface.

51. The method of claim 45 wherein the die has a first surface facing the substrate, a second surface in opposing relation to the first surface, and a sidewall between the first and second surfaces, the foil being joined to the substrate proximate the sidewall and extending across the sidewall to physically contact the second surface.

52. The method of claim 51 wherein the sidewall has a length, and wherein the foil physically contacts a predominate portion of the sidewall length.

53. The method of claim 51 wherein the sidewall has a length, and wherein the foil is spaced from a predominate portion of the sidewall length by a gap.

54. The method of claim 51 wherein the sidewall has a length, wherein the foil is spaced from a predominate portion of the sidewall length by a gap, and wherein the gap has electrically conductive epoxy extending from the sidewall to the foil.

55. The method of claim 45 wherein the metal foil is selected from the group consisting of copper foil and aluminum foil.

56. The method of claim 45 further comprising adhering the die to the substrate with an electrically conductive epoxy.

57. A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate having a pair of opposing surfaces, the surfaces being a first surface and a second surface, the circuitry being on the first surface;

adhering a metal foil to the second surface;

adhering a semiconductive-material-comprising die to the metal foil, the die having circuitry supported thereby; and

electrically connecting the circuitry supported by the die to the circuitry on the substrate with a plurality of electrical interconnects extending through the opening.

58. The method of claim 57 wherein the die has a pair of opposing sides; wherein the die covers a portion of the metal foil and leaves an other portion of the metal foil extending outwardly beyond one of the opposing sides of the die; and further comprising wrapping at least some of said other portion of the foil along the at least one of the opposing sides of the die.

59. The method of claim 58 wherein the die comprises a first surface facing the substrate and second surface in opposed relation to the first surface, the other portion of the foil being wrapped along both of the opposing sides of the die and over the second surface of the die.

60. The method of claim 57 wherein the die has a pair of opposing sides; wherein the die covers a portion of the metal foil and leaves a pair of other portions of the metal foil extending outwardly beyond the opposing sides of the die; said pair of other portions comprising a first other portion which extends outwardly of the first side of the die, and a second other portion which extends outwardly of the second side of the die; the method further comprising wrapping the first other portion of the foil along the first of the opposing sides of the die, and wrapping the second other portion of the foil along the second of the opposing sides of the die.

61. The method of claim 60 wherein die comprises a first surface facing the substrate and second surface in opposed relation to the first surface, the first and second other portions of the foil joining one another over the second surface of the die.

62. The method of claim 61 wherein the first and second other portions overlap one another over the second surface of the die.

63. A method of forming a board on chip package, comprising:

providing an insulative substrate having circuitry thereon and an opening therethrough, the substrate comprising a first surface and a second surface in opposing relation to the first surface, the circuitry being on the first surface, the substrate further comprising a cavity extending into the second surface and proximate the opening;

placing a semiconductive-material-comprising die within the cavity and electrically connecting circuitry supported by the die to the circuitry on the substrate first surface with a plurality of conductive interconnects extending through the opening, the die having an inner surface facing the substrate and an outer surface in opposing relation to the inner surface; and

placing a metal sheet outwardly of the die and in physical contact with at least a portion of the die outer surface.

64. The method of claim 63 wherein the die has a portion extending outwardly of the cavity, and wherein the sheet extends along the second surface of the substrate and over the portion of the die extending outwardly of the cavity, the method further comprising bonding the sheet to the second surface of the substrate.

65. The method of claim 63 wherein the die is entirely received in the cavity inwardly of the second surface of the substrate, and wherein the sheet extends along the second surface of the substrate and over the cavity to enclose the die in the cavity, the method further comprising bonding the sheet to the second surface of the substrate.

66. The method of claim 63 wherein the metal sheet is selected from the group consisting of copper foil and aluminum foil.

67. The method of claim 63 further comprising adhering the die to the substrate with an electrically conductive epoxy.

68. A method of forming a plurality of board on chip packages, comprising:

providing an insulative substrate having a repeating circuitry pattern thereon and a plurality of openings therethrough, the openings being in one-to-one correspondence with individual of the repeated circuitry patterns;

adhering a plurality of semiconductive-material-comprising dies to the substrate and electrically connecting circuitry supported by the dies with the circuitry on the substrate utilizing a plurality of electrical interconnects extending through the openings;

joining a metal foil to the substrate and extending the metal foil over the plurality of dies; and

cutting the substrate and metal foil to form singulated die packages comprising a single die, a portion of the substrate having a single repeated pattern of the circuitry, and a portion of the metal foil.

69. The method of claim 68 wherein the substrate comprises areas between the die, and wherein the metal foil is bonded to such areas before the cutting of the substrate.

70. The method of claim 69 wherein the bonding comprises welding the metal foil to the substrate by melting a portion of the metal foil and a portion of the substrate.

71. The method of claim 69 wherein the bonding comprises adhering the metal foil to the substrate with an adhesive.

72. The method of claim 69 wherein the bonding comprises adhering the metal foil to the substrate with an electrically conductive adhesive.

73. The method of claim 69 wherein the bonding comprises adhering the metal foil to the substrate with silver-filled epoxy.

74. The method of claim 68 wherein the substrate comprises areas between the die, and wherein the metal foil is not bonded to said areas until during or after the cutting of the substrate.

Add 27